Heterogeneously Integrated System-on-a-Chip

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Heterogeneously Integrated Microsystem-on-a-Chip

STATEMENT OF GOVERNMENT INTEREST

FIELD OF THE INVENTION

The present invention relates to microsystems packaging and, more
particularly, to an apparatus and method for integrating heterogeneous
microsystems devices on a single chip.

BACKGROUND OF THE INVENTION

Microsystems packaging involves the assembly and interconnection of
microelectronics, microelectromechanical systems (MEMS), photonics,
RF/wireless, fluidic, and other microscale devices into a system-level board or
chip to form an integrated microsystems product. Microsystems packaging must
satisfy more complex and diverse requirements than a strictly microelectronic
package. In addition to the interconnection of electrical components,
microsystems packaging requires the interconnection of actuators, sensors, and
other devices. In addition, a microsystem package must provide for
environmental protection, thermal management, mechanical support, power and
signal distribution, testing, and connection with the outside world. Therefore,
packaging often controls the microsystem's performance, cost, size, and
reliability. Portable products, in particular, are driving the development of very
dense packaging concepts comprising integrated electronic, optical, mechanical,
chemical, and biological functions. A major roadblock in developing a highly
miniaturized microsystem is the difficulty in integrating the different device
technologies in a small volume. However, packaging concepts are evolving

2

toward the full integration of a variety of functions into a complete system on a single chip.

As shown in FIG. 1, microelectronics packaging involves multiple levels of integration. A traditional circuit board **120** comprises integrated circuits (ICs) **122**

5   and passives **124** that are individually packaged, attached to a printed wiring board (PWB) **126** and interconnected by external wiring lines (e.g., copper foil tracks) on the surface of the PWB **126**. Single chip packages **132** and **136** typically comprise the electrical component, a bonding structure of the component to the package, and a means to attach the package to the PWB **126**.

10   For example, for surface mount assembly of a plastic package **132** the IC **122** can be encapsulated in a plastic **133** and wirebonded to a lead frame **134** that is solder-bonded to electrically conductive pads on the PWB **126**. In a ceramic package **136** the IC **122** can be wirebonded to a ceramic chip carrier **137** that is bonded to the PWB **126** by a ball grid array, or the like. The ceramic package

15   **136** can be hermetically sealed by a metal cap **138**. In addition to active devices, the microelectronics package can also comprise discrete and/or integrated passive devices (IPDs) **124**, such as resistors and capacitors, surface mounted in a hybrid fashion on the PWB **126**. Power can also be brought into and signals taken out of the active devices by plated through-holes or vias **128**.

20   With the PWB, the best miniaturization that can be achieved provides a footprint that is the sum-total of the single-chip packages, passives, and interconnection areas. Furthermore, the high frequency electrical performance of in-plane hybrid circuits can be degraded, as a result of transmission line effects and circuit parasitics, thus limiting such packages for RF applications. In

25   addition, wirebonds or solder joints pose a major reliability concern in such hybrid packages.

At the next level of integration, a multichip module (MCM) **140** comprises bare chips **122** and passives **124** mounted directly to a common substrate/package structure that replaces the chip-level packaging of the

30   traditional circuit board. The MCM substrate **146** can comprise a deposited metal/dielectric multilayer structure on a base layer, a thick-film or cofired

multilayer ceramic, or an organic laminate multilayer structure. The MCM substrate **146** provides signal input/output connections for the chips, signal interconnection through conducting layers **148** sandwiched between the multilayer dielectric structure, thermal management, mechanical support, and

5   environmental protection. The bare chips **122** can be placed close together and directly bonded to the substrate **146** by the use of flip chip or other direct chip attach technology. This saves the weight and volume of individual chip packaging, significantly reducing the footprint of the MCM **140**. The MCM **140** can be hermetically sealed in ceramic or metal packages or encapsulated in

10   plastic (not shown). The MCM **140** typically enables a higher packaging efficiency, better electrical performance, greater reliability, and lower cost than the traditional circuit board **120**.

As an approach to building a more compact, three-dimensional (3D) package, integrated substrate technology **160** uses passives that are embedded

15   (i.e., integral passives **168**) as part of the fabrication of the multilayer substrate **166**. Bare chips **122** can be assembled directly above the embedded passives **168**, shortening interconnection distances and thereby further improving electrical performance and enabling higher packaging efficiency, lower assembly costs, and small size and weight. However, such integral substrates **166** require

20   new designs, test systems, manufacturing processes, and materials and can therefore by more costly to develop and have a longer time-to-market than with PWB or MCM packages **120** or **140**.

Fully 3D integration of components is being developed, as a result of the increasing demand for portability and miniaturization. Therefore, the longer-term

25   goal of modern packaging is the system-on-chip (SOC) **180**. Hybrid SOC packaging uses thinned silicon chips that are stacked on top of a bottom wafer of normal thickness and interconnected by vertical electrical connections. Therefore, the SOC package can provide a high level of vertical integration and interconnection, such that the package footprint is the size of the largest

30   component. In addition, stacking and interchip wiring may provide improvements in performance and reliability. In particular, interconnect delays can be

dramatically reduced by replacing long in-plane interconnects with through-wafer via interconnects.

There are several hybrid SOC packaging concepts being developed worldwide. One approach uses a modification of MCM packaging technology. In

5   this stacked MCM approach, multiple physical layers are built-up, starting with a first physical layer comprising thinned dies mounted on a substrate carrier. The in-layer dies can be interconnected with several metal deposition and etching steps, using spin-on polymer with corresponding via formation. Additional physical layers are then built up from an insulating and planarizing polymer layer

10   on the first physical layer. While providing many of the advantages of the MCM packaging in a stacked 3D package, handling thin dies can be challenging and parallel assembly of individual chips does not provide the efficiencies of wafer-level packaging. *See* Vendier *et al.*, "Ultra Thin Electronics for Space Applications," Proc. 2001 Electronic Components and Technology Conference

15   (2001), which is incorporated by reference.

Another SOC concept uses flip-chip interconnection to build a chip-on-chip (COC) structure. With the COC structure, through-hole copper electrodes on the periphery of thinned silicon chips are connected to electroplated gold micro bumps on the underlying wafer by thermal compression flip-chip bonding. The

20   narrow gap between the stacked chips is then encapsulated with an epoxy underfill resin having a low coefficient of thermal expansion (CTE) that is filled with hyperfine filler particles to reduce the thermal stress of the micro bumps. Using these techniques, the micro bumps can have a pitch of about 20 microns and the interchip wiring length can be short. However, the chips are stacked

25   after dicing, rather than at the wafer level, and the thermocompression bonding process can require relatively high temperatures and bonding forces. *See* Tomita *et al.*, "Advanced Packaging Technologies on 3D Stacked LSI utilizing the Micro Interconnections and the Layered Microthin Encapsulation," Proc. 2001 Electronic Components and Technology Conference (2001); Takahashi *et al.*,

30   "Development of Advanced 3D Chip Stacking Technology with Ultra-Fine Interconnections," Proc. 2001 Electronic Components and Technology

Conference (2001); and Umemoto *et al.*, "Superfine Flip-Chip Interconnection in 20μm-Pitch Utilizing Reliable Microthin Underfill Technology for 3D Stacked LSI," Proc. 2002 Electronic Components and Technology Conference, 1454 (2002), which are incorporated herein by reference.

5   Recently, vertically integrated circuits have been fabricated at the wafer level using stacking of thinned wafers and vertical interchip wiring. Vertical electrical connections are formed between the uppermost metal layers of the bonded wafers by fabrication and metal refill of high aspect ratio interchip vias. However, this requires that the I/O pads of the adjoining stacked wafers be

10   precisely located over each other to make the vertical electrical connections. Therefore, the bonding process requires a precise optically adjusted alignment process to carefully adjust the lithographic levels of the top and bottom wafers. Furthermore, the process uses polyimide as the intermediate glue layer. Polyimide requires a high temperature cure (i.e., about 380 °C), is hydrophilic

15   (i.e., moisture absorption of about 2%), and is conformal, necessitating that the polyimide be coated on a relatively featureless bottom wafer surface. Finally, this process does not provide for the inclusion of additional interconnect circuitry and passives in the intermediate layer. *See* Ramm *et al.*, "Three dimensional metallization for vertically integrated circuits," Microelectronic Engineering 37/38,

20   39 (1997), which is incorporated herein by reference.

        The microsystem-on-a-chip (μSOC) technology of the present invention addresses the need for heterogeneously integrated, ultra-miniaturized, higher performing, robust and cost-effective microsystem package. The μSOC is a modular, multi-function, multi-chip stacked package that provides all of the

25   needed system-level functions. A highly integrated microsystem package, comprising electronics, sensors, optics, and MEMS, can be miniaturized both in volume and footprint to the size of a bottle-cap or less. Furthermore, the μSOC package eliminates the use of wirebonds and solder joints, thus making the package inherently more robust for applications exposed to extreme mechanical

30   shock and vibration environments. The μSOC package will enable wireless distributed sensor systems comprising miniaturized, unattended, unobtrusive,

surveillance devices for monitoring for military battlefields, infrastructure systems, and manufacturing processes.

SUMMARY OF THE INVENTION

The present invention is directed to a microsystem-on-a-chip, comprising
5   a bottom chip comprising one or more microsystem devices with associated input/output pads on the top surface of the bottom chip; an interconnect layer on the top surface of the bottom chip, the interconnect layer comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture
10   pads connected to the associated input/output pads on the top surface of the bottom chip; and a thin upper chip on the interconnect layer, the thin upper chip comprising one or more microsystem devices with associated input/output pads on the top surface of the thin upper chip that are connected to the one or more via capture pads in the interconnect layer by conductive vias through the thin
15   upper chip. The microsystem-on-a-chip of can further comprise at least one additional stacked layer on the thin chip. The interconnect layer can further comprise at least one passive component, such as a thin-film resistor, multi-layer capacitor, or spiral inductor. The compliant dielectric material can be an organic polymer, such as benzocyclobutene.
20   The present invention further includes a method for fabricating a plurality of microsystems-on-a-chip, comprising providing a bottom wafer comprising a plurality of chips, each chip comprising one or more microsystem devices with associated input/output pads on the top surface of the bottom wafer; forming an interconnect layer on the top surface of the bottom wafer, the interconnect layer
25   comprising a compliant dielectric material and an interconnect structure embedded in the compliant dielectric material, the interconnect structure comprising one or more via capture pads connected to the associated input/output pads on the top surface of the bottom wafer; bonding a thin upper wafer to the interconnect layer, the thin upper wafer comprising a plurality of
30   chips, each chip comprising one or more microsystem devices with associated

7

input/output pads on the top surface of the thin upper wafer that are connected to the one or more via capture pads in the interconnect layer by conductive vias through the thin upper wafer; and singulating the plurality of chips from the bottom wafer, the interconnect layer and the thin wafer. The interconnection vias

5   can be fabricated either before, or after, the wafers are bonded together.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form part of the specification, illustrate the present invention and, together with the description, describe the invention. In the drawings, like elements are referred to

10   by like numbers.

FIG. 1 shows a schematic illustration of a several microelectronics packaging concepts.

FIG. 2 shows a schematic illustration of the microsystem-on-a-chip package.

15   FIG. 3 shows a cross-sectional side view of a singulated chip from the bottom two wafers in a multi-wafer stack.

FIGs. 4A – 4E show a wafer-stacking method wherein interchip vias are formed prior to the bonding of the two wafers together.

FIGs. 5A – 5G show a method to thin an upper wafer and bond the

20   thinned upper wafer to a bottom wafer.

FIGs. 6A – 6E show a wafer-stacking method wherein interchip vias are formed after the two wafers are bonded together.

DETAILED DESCRIPTION OF THE INVENTION

In FIG. 2 is shown an example of the microsystem-on-a-chip package of

25   the present invention in which different device technologies can be heterogeneously integrated in a 3D stack as a single chip. The stacking method can be used to integrate widely different materials used in the IC and MEMS industries, such as silicon, compound semiconductors, glass, and ceramics, and different types of devices like CMOS, memory, photonic, sensors, RF and

passive components by a batch process at the wafer level. Any significant stresses associated with thermal expansion mismatch between different materials in the layers of the stack **200** can potentially cause delamination, cracking or bending. Therefore, a bottom wafer **220** of normal thickness can be

5   a relatively rigid and the stacked wafers **240** can be thin so that their individual contribution to thermal expansion mismatch stresses are minimal. On top of the bottom wafer **220**, the series of thinned wafers **240** can be stacked, glued and electrically interconnected. An interconnect layer **230** between each wafer provides additional compliance to the stacked structure **200**. Therefore, a

10   thinned wafer fabricated in one technology can be wafer-level attached on top of another wafer fabricated in another technology. Preferably, the top wafer can be a sensor layer to enable probing of the external environment in order to measure a chemical, biological, or physical effect. The on-board circuitry can be buried in the stack for environmental protection and low-loss signal propagation.

15   The wafer stack **200** can be singulated into single chips **180** by standard dicing methods. Each 3D stacked chip **180** can be a self-contained microsystem having approximately the same area and volume as a single IC. The top or the bottom surface of the stacked chip **180**, if needed, can be made available for attachment of discrete devices, MEMS, batteries, antennas or commercial-off-

20   the-shelf (COTS) surface mount components. The modular 3D stack achieves the goals of monolithic integration at a small fraction of the cost of conventional microsystems packaging. In particular, since it is a wafer-level process, the processing cost per die is minimal.

       In FIG. 3 is shown a cross-sectional side view of a portion of the bottom

25   two wafers **220** and **240** of the multi-wafer stack **200** that can be singulated into a single chip **180**. Each wafer **220** and **240** can have one or more microsystems devices **222** and **242** per chip with associated input/output (I/O) pads **223** and **243** on the uppermost surfaces of the wafers **220** and **240**. The bottom wafer **220** can comprise silicon, alumina, or a low-temperature co-fired ceramic (LTCC)

30   of normal thickness (e.g., 600 microns thickness). The upper thinned wafer **240** (e.g., 20 to 120 microns thickness) comprises a plurality of conductive through

vias **244** that enable vertical, interchip electrical connection. The interconnect layer **230** comprises a compliant dielectric material **231** that attaches the two wafers **220** and **240**. The interconnect layer **230** further comprises a high-density interconnect structure embedded in the dielectric material **231** that is electrically

5   connected to the conductive interchip vias **244** and allows signal redistribution between the I/O pads **223** and **243** of the upper and bottom wafers **220** and **240**. This interconnect structure comprises via capture pads **232** that enable the wafers to be stacked without requiring the I/O pads **223** and **243** of adjoining wafers to be located over each other. Furthermore, passive components **238**,

10   comprising thin film resistors, capacitors, and inductors, can be embedded in the interconnect layer **230** to provide greater flexibility and further miniaturization than is possible with discrete passive components.

The interconnect layer **230** comprises a compliant dielectric material **231** that can be used to glue the two wafers **220** and **240** together. The compliant

15   dielectric material **231** is preferably a polymer. The polymer should provide adhesion of the two adjoining wafers and should be able to withstand the mechanical, thermal, and chemical conditions encountered during the subsequent wafer stacking processes. Furthermore, the thickness of the interconnect layer **230** should be thin, preferably less than about 50 microns, yet

20   thick enough to reduce residual stress and provide adequate insulation and planarization of the underlying topology.

The polymer is preferably benzocyclobutene (BCB). BCB is a thermosetting polymer that is inert to most chemicals, can be used with a variety of substrate materials, and has very good spin-on planarization, good adhesion,

25   low susceptibility to cracking, and low moisture absorption. BCB has a glass transition temperature of about 350 °C, providing good long-term stability. The bonding temperature can be below 250 °C, so that the packaging method is compatible with CMOS circuitry. Because BCB is self-planarizing, surface planarity of the interconnect layer can be better than that obtained with a

30   conformal coating. This property is desirable for smoothing the rough topology provided by the microsystems devices **222**, embedded passives **238**, and

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interconnect circuitry **223** and **232**, enabling the void-free stacking of multiple wafers. In addition, BCB has a relatively low dielectric constant (i.e., about 2.65), enabling high speed signal propagation and reduced capacitive coupling and cross-talk between the interconnection lines. Although the use of any organic

5   polymer as a glue layer prevents a truly hermetic package, BCB absorbs almost an order of magnitude less moisture in humid environments then polyimide. Other compliant dielectric materials, including inorganics and organic/inorgranic hybrids, can also be used to bond the wafers together, depending on the application and processing requirements.

10   The interconnect layer **230** further comprises a multilayer, high-density interconnect structure embedded in the dielectric glue material **231** that allows signal redistribution between the I/O pads **223** and **243** on the uppermost surfaces of the two wafers **220** and **240**. Electrically conducting interchip vias **244** provide vertical electrical connections between the stacked devices.

15   Because the stacked wafers are thin, the vias can have a low aspect ratio that can still be easily metallized. The vias **244** can be insulated from the wafer material **241** with a dielectric coating **245** and filled with a conducting material (e.g., a metal) **246**. Because of the difficulty in aligning all of the vias **244** between multiple stacked wafers having very high I/O density devices, the

20   interconnect structure can comprise large via capture pads **232** on the lower wafer **220**. The size of these via capture pads **232** can be adjusted to control the alignment tolerance. The interconnect structure can be fabricated using a good electrical conductor, such as copper, to provide for fast signal speed and low power dissipation.

25   The interconnect layer **230** can also accommodate embedded passive components **238**, such as resistors, capacitors and inductors. Thin film resistors can comprise patterned layers of resistive material embedded in the interconnect dielectric **231** and electrically connected to the interconnect structure. Embedded capacitors can be built in polymer/copper multi-layers by sandwiching

30   layers of dielectric between copper electrodes. Inductors can comprises 2D and 3D spiral structures made of copper embedded in the interconnect dielectric **231**.

11

The fabrication method of the present invention uses an aligned bonding process for wafer-level stacking of devices with interchip via connection and with capability to reroute interconnections between levels. The method does not require any extreme temperature, pressure, voltage or chemical environment.

5 The method comprises wafer thinning and handling, interconnect layer formation, aligning and bonding of the two wafers, and interchip via formation and metallization to provide electrical interconnection between the wafers in the vertical stack. The aligned bonding process preferably comprises bonding the wafers together with an polymeric dielectric, such as BCB, as a glue. The

10 interconnection vias can be fabricated either before, or after, the wafers are bonded together.

In FIGs. 4A-4E is shown a wafer-stacking method wherein the interchip vias are fabricated prior to bonding of the wafers together.

In FIG. 4A, a bottom wafer **220** and an upper wafer **240** each comprise

15 one or more devices **222** and **242** with associated I/O pads **223** and **243** constructed on the top surface of a thick wafer.

In FIG. 4B, blind via holes **247** are formed that extend from the I/O pads **243** on the top surface to part way through the thick upper wafer **240**. The blind vias **247** can extend to a depth greater than the final thickness of the upper wafer

20 **240** after thinning. The blind vias **247** can be formed by a variety of directional etching processes, such as reactive ion etching, Bosch etching, or laser drilling. These techniques can typically provide vias with diameters of about 25 microns on a pitch of 50 microns, enabling high-density interconnections.

The interconnect layer **230** on the bottom wafer **220** comprises the

25 dielectric glue material, the interconnect structure, and embedded passives. The dielectric glue material **231** can be coated on the top surface of the bottom wafer **220** to encapsulate the interconnect structure and enable bonding to the upper wafer **240**. For example, the glue material **231** can comprise BCB polymer that is spun-on the topside of the bottom wafer **220**. The BCB layer can be

30 photodefinable or non-photodefinable (i.e., dry-etchable). Both the photosensitive and dry-etch grades are marketed as CYCLOTENE™ advanced

electronic resins by the Dow Chemical Company. Photodefinable BCB is a negative acting photopolymer whereby the unexposed regions can be removed by a suitable developer. Each BCB layer of the multilayer interconnect structure can typically be 1 to 25 microns. Total BCB multilayer thickness can be about 50

5 microns or less.

The interconnect structure can comprise multiple patterned metal layers sandwiched between the dielectric layers. The conductor of the interconnect structure can comprise a thin titanium adhesion layer (e.g., 20 nm thickness) and a 2 to 20 microns thickness copper layer, depending on the thickness of the BCB

10 layer. The copper lines can be patterned by etching, lift-off, or other patterning method. Via capture pads **232** can be formed in the interconnect layer **230** to align with the vias **244** from the upper wafer **240** and to redistribute the signals from the I/O pads **243** on the upper wafer with the I/O pads **223** on the bottom wafer. The size of the via capture pads **232** can be adjusted to control the

15 alignment tolerance.

A process for building up a copper interconnect structure within a BCB intermediate layer is described by Strandjord *et al.*, "Process Optimization and Systems Integration of a Copper / Photosensitive Benzocyclobutene MCM-D: Dielectric Processing, Metallization, Solder Bumping, Device Assembly, and

20 Testing," <u>Int. J. Microcircuits and Electronic Packaging</u> <u>19</u>(3), 260 (1996), which is incorporated herein by reference. The process used up to five metal layers embedded in sequentially deposited thin layers of photodefinable BCB. The process includes preparation of a wafer surface for reliable BCB bonding, spin-coating of a photosensitive BCB layer on the wafer surface, pre-exposure baking

25 of the coated BCB at a low temperature, photolithography of the negative BCB layer, solvent development of the BCB resist material to form vias, soft-curing of the BCB to eliminate cracking and ensure resistance to subsequent processing, application and photolithography of a lift-off photoresist, copper metallization by evaporation, and solvent liftoff after metallization to provide the interconnect

30 metal lines and via pads. The layer thickness of the photo-BCB was about 5 microns. Multiple layers of BCB polymer and metal can be built-up using this

13

process. Layer-to-layer electrical connections can be accomplished with the metallized vias in the BCB layers onto metal capture pads in the underlying BCB layer. After build-up, the multiple layers can be hard-cured in an oven.

Thicker BCB layers may be desirable for some applications, for example

5   to minimize insertion losses in RF circuits and maximize miniaturization. Thicker BCB layers (e.g., 20 microns) can be made with a non-photodefinable BCB that can be patterned by dry etching. The BCB in the exposed areas can be selectively removed to make the vias and streets by reactive ion etching (RIE) with an oxygen/fluorine mixture. The photolithographic pattern can be defined

10   either by a hard mask (e.g., aluminum) or a soft mask (e.g., photoresist).

Embedded passives can be incorporated in the metal layers of the interconnect structure. For example, thin film resistors can be made of tantalum nitride (TaN), tantalum silicide (TaSi), nichrome (NiCr), or chrome silicide (CrSi). The resistivity can be varied by changing the composition, thickness, or meander

15   pattern of the resistor. Typical embedded resistors have resistances of 10 – 10,000 ohms. Embedded capacitors can be built in BCB/copper multi-layers by sandwiching layers of Ta/Ta_2O_5 dielectric between copper electrodes. The capacitance can be varied by changing the capacitor area. Capacitance values of 50 pF to 100 nF at 1 –100 MHz are typical. Smaller capacitors, less than

20   about 1 nF, behave as lumped elements at less than about 100 MHz. Inductors can comprise 2D and 3D spiral structures made of copper embedded in the BCB dielectric. These spiral inductors behave as lumped elements with inductances of 1 to 40 nH at low frequencies. For higher frequencies (e.g., greater than 4 GHz), transmission lines can be used as inductors. Tolerance for most of these

25   embedded passives can be less than +/- 4%. *See, e.g.,* T. Lenihan *et al.*, "Thin Film Resistors, Capacitors, and Inductors in Flexible Polyimide Films," Proc. 1996 Electronic Components and Tech. Conf., pp. 119-124, Orlando, May 28-31 (1996); R. Kambe *et al.*, "Copper-Polyimide Multilayer Substrates for High Speed Signal Transmission," Proc. 41st ECTC Conf., pp. 14-16 (1991); and R. R. Kola *et*

30   *al.*, "Thin Film Resistors and Capacitors for Advanced Packaging," Proc. 3rd Int.

<u>Symposium on Adv. Packaging Materials</u>, Atlanta, pp. 71-74 (1997); which are incorporated herein by reference.

     In FIG. 4C, the bottom side of the upper wafer **240** is partially removed to convert the blind via holes to through vias **247** and provide a thin, flexible upper

5   wafer **240**. The thinned upper wafer **240** can be aligned with and bonded to the planarized interconnect layer **230** on the bottom wafer **220** with the aid of a supporting carrier wafer **250** that is attached to the upper wafer **240** with an adhesive **252**, according to the aligned bonding process described below.

     In FIGs. 5A – 5G is shown an aligned bonding process to thin the upper

10   wafer **240** and bond the thinned upper wafer **240** to the bottom wafer **220**.

     In FIG. 5A is shown a carrier wafer **250**, a double-sided adhesive tape **252**, and the upper wafer **240** to be thinned. The carrier wafer **250** can be, for example, a planar glass wafer. The use of the carrier wafer **250** enables the upper wafer **240** to be handled similarly to a rigid, thick wafer during thinning and

15   subsequent wafer bonding. The adhesive tape **252** can be a thermal self-release adhesive tape that allows the carrier wafer **250** to be cleanly and easily bonded and then de-bonded from the upper wafer **240** without affecting other materials used in the wafer bonding method. For example, the adhesive tape can be REVALPHA™ thermal release tape, manufactured by Nitto Denko, Inc. The

20   REVALPHA™ tape has tiny gas bubbles that are entrapped in a polymeric adhesive. When the tape is heated above a self-release temperature, the trapped air bubbles expand, forcing the joined wafers to break loose. Therefore, the wafer release occurs without the application of additional applied force. Furthermore, the self-release process leaves no visual residue on the released

25   surface of the upper wafer. The REVALPHA™ tapes are available with self-release temperatures of 90 to 170 °C.

     In FIG. 5B, the carrier wafer **250** is attached to the top surface of the upper wafer **240** (i.e., the upper wafer devices are not shown) using the adhesive tape **252**. The attachment is preferably done in a clean room environment to

30   prevent the entrapment of particulates that may create a hole or other damage to the upper wafer **240** when it is thinned.

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In FIG. 5C, the exposed bottom surface of the upper wafer **240** is thinned while being supported by the carrier wafer **250**. The upper wafer **240** can be thinned (e.g., 20 to 120 microns thickness) by grinding, lapping, and/or polishing.

In FIG. 5D, the bottom surface of the thinned, carrier-supported upper

5   wafer **240** is bonded to the planarized interconnect layer **230** on the top surface of the bottom wafer **220** (i.e., the bottom wafer devices are not shown). A low-temperature process using a polymer to bond wafers has been described by Niklaus *et al.*, "Low-temperature full wafer adhesive bonding," J. Micromech. Microeng. 11, 100 (2001), which is incorporated herein by reference. Niklaus

10   found that the polymer material, the bonding pressure, and the pre-curing time and temperature for the polymer significantly influence void formation at the bond interface. In the present invention, a similar low-temperature bonding process can be used to bond a thinned upper wafer, bonded to a carrier wafer with the thermal release tape, to the BCB interconnect layer on the bottom wafer.

15   Excellent void-free and strong bonds have been achieved by bonding the carrier-supported upper wafer to the BCB-coated bottom wafer at temperatures of 80 to 150 °C.

Preferably, the wafers **220** and **240** can be bonded in a wafer-bonding machine. The wafers can be heated to a temperature slightly below the self-

20   release temperature of the thermal release tape (e.g., to below 90 to 170 °C) and the wafer bonding machine chamber can be evacuated. The wafers are preferably bonded, starting from the center of the aligned wafers and proceeding outwardly to the edges. This center-first bonding can be facilitated by the use of spacers situated around the periphery and between the to-be-bonded wafer

25   surfaces. The spacers can be removed as the bonding force is applied outwardly.

As shown in FIG. 5E, this process results in a uniform bond of the wafer surfaces together without trapping air bubbles. Acoustic imaging has shown the absence of air voids in the bond region when this method is used to bond the

30   wafers **220** and **240**.

In FIG. 5F, the carrier wafer **250** and the adhesive tape **252** are released from the top surface of the upper wafer **240** by heating to a temperature in excess of the self-release temperature (e.g., to greater than 90 to 170 °C).

As shown in FIG. 5G, removal of the carrier wafer and adhesive provides

5   the thinned upper wafer **240** bonded to the interconnect layer **230** of the thick bottom wafer **220**. The bonded wafer stack can then be further processed.

Returning now to FIG. 4D, after the thinned upper wafer **240** is bonded to the thick bottom wafer **220** and the carrier wafer **250** is removed, the BCB interconnect layer material **231** can be soft cured at about 210 °C to further

10   eliminate any air voids. The vias **247** can be then be further etched through the BCB **231**, using the via holes in the upper wafer **240** as a mask, stopping at the via capture pads **232** in the interconnect layer **230**.

In FIG. 4E, the vias **244** can be coated with an insulating dielectric **245** and filled with a metal **246** to form a conducting plug. A suitable process for

15   forming hollow vias, deposition of a insulating dielectric coating and seed layers on the interior surface of the hollow vias, and copper plating of the vias is described by Spiesshoefer *et al.*, "IC Stacking Technology using Fine Pitch, Nanoscale through Silicon Vias," Proc. 2003 Electronic Components And Technology Conference, 631 (2003), which is incorporated herein by reference.

20   The hollow vias are first cleaned to provide a pristine surface for subsequent insulating and metal layer depositions. The insulating dielectric coating **245** can be formed on the inside of the hollow vias to electrically isolate the metallized vias from the upper wafer material. The dielectric coating **245** can be, for example, silicon dioxide or BCB. Finally, conducting vias **244** can be formed

25   through the upper wafer **240** and partially through the insulating layer **230** by metallization **246** of the via, for example using evaporative or electroplated copper. The metallized vias **244** thereby electrically connect the I/O pads **243** of the devices of the upper wafer **240** to the I/O pads **223** of the devices of the bottom wafer **220** by way of the via capture pads **232**.

30   In FIGs. 6A – 6E is shown a wafer-stacking method wherein the interchip vias are formed after the wafers are bonded, using the processes described

above. In FIG. 6A is shown a bottom wafer **220** and an upper wafer **240**, each comprising one or more devices **222** and **242** with associated I/O pads **223** and **243** constructed on the top surface of a thick wafer. In FIG. 6B, the interconnect layer **230** is formed on the bottom wafer **220**, comprising an interconnect

5   structure that is encapsulated in the interconnect layer material **231**. In FIG. 6C, the carrier-supported thinned upper wafer **240** is aligned and bonded to the top surface of the planarized interconnect layer **230** on the bottom wafer **220**. In FIG. 6D, hollow vias **247** are formed that extend from the I/O pads **243** on the top surface of the bonded upper wafer **240** through to the via capture pads **232** in the

10   interconnect layer **230**. In Fig. 6E, the hollow vias **247** are lined with a dielectric coating **245** and filled with a metal **246** to form metallized vias **244** that provide an electrical connection from the I/O pads **243** of the upper wafer **240** to the I/O pads **223** of the bottom wafer **220**.

Additional thinned wafers can be built up on top of the two-wafer stack by

15   a similar wafer-stacking method. After stacking, individual chips can be separated from the stacked wafers using a standard wafer-dicing process. The separated dies can withstand normal next board-level assembly processes including high temperature solder reflow process, requiring thermal treatment at about 310 °C for a few minutes.

20   The present invention has been described as a microsystem-on-a-chip package and a wafer-stacking method to assemble a microsystem-on-a-chip. It will be understood that the above description is merely illustrative of the applications of the principles of the present invention, the scope of which is to be determined by the claims viewed in light of the specification. Other variants and

25   modifications of the invention will be apparent to those of skill in the art.